CLAIMS

1. A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to memory cells in at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

2. The memory module of claim 1 wherein the link interface comprises an optical input/output port.

3. The memory module of claim 1 wherein the memory device interface comprises a memory controller, and the performance counter is coupled to the memory controller.

4. The memory module of claim 1 wherein the memory device interface comprises a cache, and the performance counter is coupled to the cache.

5. The memory module of claim 1 wherein the memory hub further comprises a prefetch buffer, and the performance counter is further coupled to the prefetch buffer.

6. The memory module of claim 1 wherein the memory hub further comprises a maintenance bus, and the performance counter is further coupled to the maintenance bus.

7. The memory module of claim 1 wherein the performance counter is further coupled to the link interface.

8. The memory module of claim 1 wherein the performance metric tracked by the performance counter comprises at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number.

9. The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

10. The memory module of claim 1 wherein the performance metric tracked by the performance counter comprises a performance metric related to the coupling of memory requests and data through the memory hub.

11. A memory hub, comprising:

a link interface receiving memory requests for access to memory cells in at least one of a plurality of memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

12. The memory hub of claim 11 wherein the link interface comprises an optical input/output port.

13. The memory hub of claim 11 wherein the memory device interface comprises a memory controller, and the performance counter is coupled to the memory controller.

14. The memory hub of claim 11 wherein the memory device interface comprises a cache, and the performance counter is coupled to the cache.

15. The memory hub of claim 11, further comprising a prefetch buffer, and wherein the performance counter is further coupled to the prefetch buffer.

16. The memory hub of claim 11, further comprising a maintenance bus, and wherein the performance counter is further coupled to the maintenance bus.

17. The memory hub of claim 11, wherein the performance counter is further coupled to the link interface.

18. The memory hub of claim 11 wherein the performance metric tracked by the performance counter comprises at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number.

19. The memory hub of claim 11 wherein the performance metric tracked by the performance counter comprises a performance metric related to the coupling of memory requests and data through the memory hub.

20. The memory hub of claim 11 wherein the memory devices comprise dynamic random access memory devices.

21. A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to memory cells in at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to couple memory requests to the memory devices for access to memory cells in at least one of the memory devices and to receive read data responsive to at least some of the memory requests; and

a performance counter coupled to the memory device interface, the performance counter operable to track at least one performance metric.

22. The computer system of claim 21 wherein the link interface comprises an optical input/output port.

23. The computer system of claim 21 wherein the memory device interface comprises a memory controller, and the performance counter is coupled to the memory controller.

24. The computer system of claim 21 wherein the memory device interface comprises a cache, and the performance counter is coupled to the cache.

25. The computer system of claim 21 wherein the memory hub further comprises a prefetch buffer, and the performance counter is further coupled to the prefetch buffer.

26. The computer system of claim 21 wherein the memory hub further comprises a maintenance bus, and the performance counter is further coupled to the maintenance bus.

27. The computer system of claim 21 wherein the performance counter is further coupled to the link interface.

28. The computer system of claim 21 wherein the performance metric tracked by the performance counter comprises at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number.

29. The computer system of claim 21 wherein the memory devices comprise dynamic random access memory devices.

30. The computer system of claim 21 wherein the performance metric tracked by the performance counter comprises a performance metric related to the coupling of memory requests and data through the memory hub.

31. A method of reading data from a memory module, comprising:

receiving memory requests for access to a memory device mounted on the memory module;

coupling the memory requests to the memory device responsive to the received memory request, at least some of the memory requests being memory requests to read data;

receiving read data responsive to the read memory requests; and

tracking at least one performance metric within the memory module.

32. The method of claim 31 wherein the act of tracking at least one performance metric comprises tracking at least one performance metric selected from the group consisting of page hit rate, number or percentage of prefetch hits, cache hit rate or percentage, read rate, number of read requests, write rate, number of write requests, rate or percentage of memory bus utilization, local hub request rate or number, and remote hub request rate or number.

33. The method of claim 31 wherein the act of tracking at least one performance metric comprises tracking a performance metric related to the coupling of memory requests and data through the memory hub.

34. The method of claim 31 wherein the act of receiving memory requests for access to a memory device mounted on the memory module comprises receiving optical signals corresponding to the memory requests.